

## 1. Description

The core is based on the original core for the 8051 and was captured and verified by new design methods in a modular structure as IP cell. It can be synthesized and implemented in any ASIC structure with peripheral integrated logic and analog circuitry.

### Typical main parameters

- instruction cycle typical 1  $\mu$ s at 12 MHz (depending on technology and spec requirement)
- variable number of I/O-ports (scalable)
- 128 Bytes of internal RAM
  - 32 Byte bank-register
  - 16 Byte bit-addressable RAM
  - 80 Byte general purpose RAM
- 21 special function registers (SFR)
  - more can be added, e.g. for additional ports
- internal and/or external program memory up to 64 k Bytes
- external data memory of up to 64 k Bytes
- 5 interrupt sources in two priority levels
  - external interrupt 0/1
  - timer/counter interrupt 0/1
  - serial interface interrupt
- other interrupt sources can be added
- serial interface with variable Baud-rate
- two 16-bit timers/counters

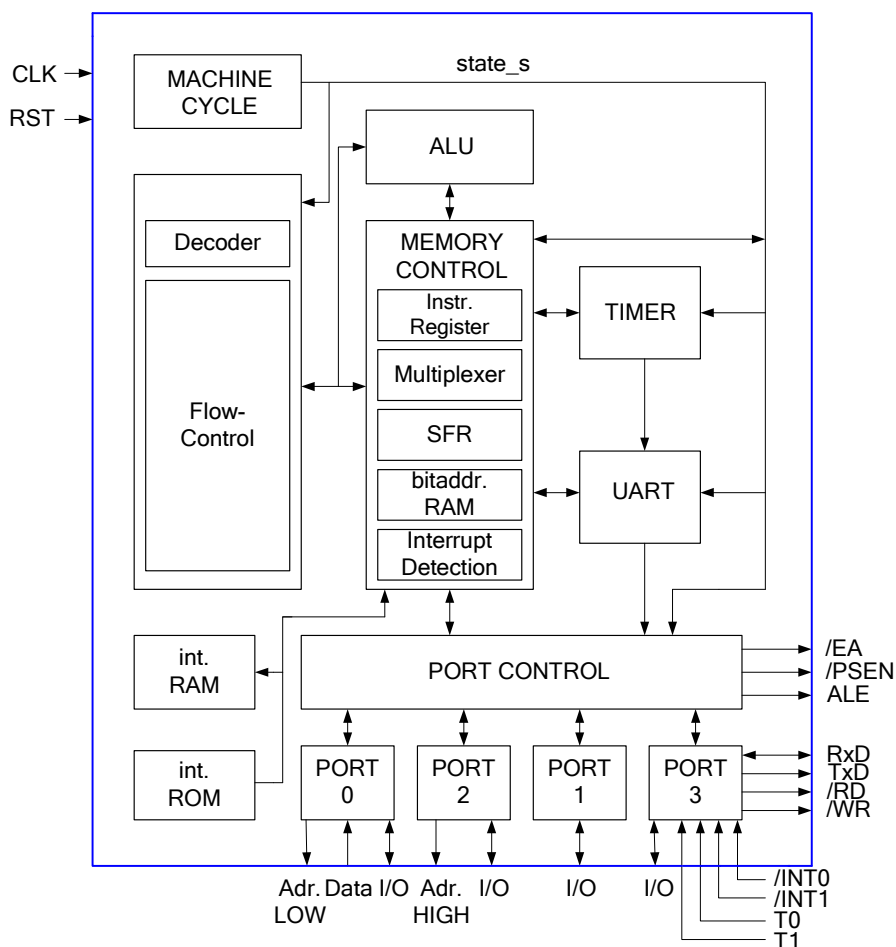


Figure 1: Typical functional block diagram

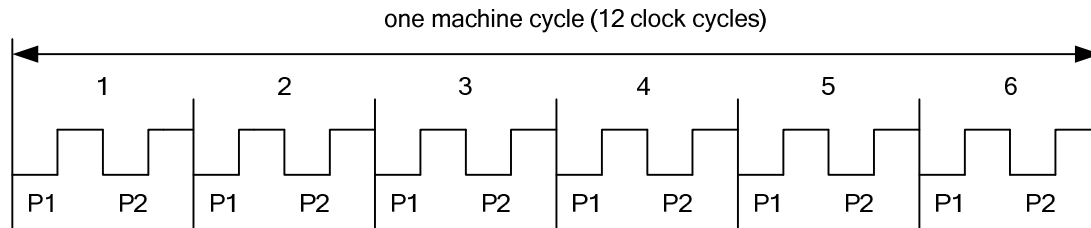


## 2. Port Description

CLK	Clock ( <i>input</i> )
RST	Reset ( <i>input</i> )
$\overline{\text{EA}}$	External Access ( <i>input</i> ). If the pin is low, the program is executed only from external memory. (low active)
ALE	Address Latch Enable ( <i>output</i> ). ALE is the signal that latches the address into an external register during the first half of a memory cycle. The ALE pulses at rate of 1/6 oscillator frequency and can be used as a general purpose clock.
$\overline{\text{PSEN}}$	Program Store Enable ( <i>input</i> ). It is a control signal that enables external program memory. (low active)
Port 0	( <i>input/output</i> ) Port 0 is a dual-purpose port. It is used as a general purpose I/O port. For designs with external memory it is used for a multiplexed address and data bus.
Port 1	( <i>input/output</i> ) Port 1 is a dedicated I/O port.
Port 2	( <i>input/output</i> ) Port 2 is a dual-purpose port serving as general purpose I/O or as the higher byte of the address bus for designs with external memory.
Port 3	( <i>input/output</i> ) Port 3 is a dual-purpose port as well as general purpose I/O. This port is multifunctional with an alternate purpose related to special features of the 8051. The alternate purposes of the Port 3 pins are:
$\overline{\text{WR}}$	external data memory write strobe ( <i>output</i> )
$\overline{\text{RD}}$	external data memory read strobe ( <i>output</i> )
RxD	receive data for serial interface ( <i>input/output</i> )
TxD	transmit data for serial interface ( <i>input/output</i> )
$\overline{\text{INT0}}$	external interrupt 0 ( <i>input</i> )
$\overline{\text{INT1}}$	external interrupt 1 ( <i>input</i> )
T0	timer 0 external input ( <i>input</i> )
T1	timer 0 external input ( <i>input</i> )

### 3. Machine Cycle

The 8051 controller needs 12 clock cycles for one machine cycle. Processing of program instructions takes place according to a program sequence pattern specified for each instruction. This determines the run time of the individual instructions with the processor clock. The 12 clock cycles are divided in 6 groups of conditions. Two clock cycles are assigned to each group of conditions.



**Figure 2: Machine cycle**

The block MACHINE CYCLE derives the individual conditions **Z1\_P1** to **Z6\_P2** from the clock. The signal **state\_s** is used in other blocks as an enable signal.

### 4. Arithmetic-Logic-Unit (ALU)

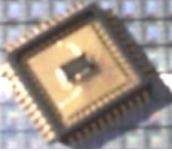
The arithmetic and logical instructions are executed in the ALU. Functions performed by the ALU include subtraction, addition, multiplication, division, logical AND, logical OR, logical XOR as well as comparison and left or right shifts.

The block **ALU** is composed of:

- **ALU\_ADD\_SUB** for addition and subtraction
- **ALU\_MUL** for multiplication
- **ALU\_DIV** for division
- **ALU\_LOG** for logical operations
- **ALU\_DA** for decimal adjust
- **ALU\_MUX** to the control of the individual blocks

If necessary a basic controller with simple instruction subsets or with minimum chip area (ASIC) and/or component number (FPGA) can be synthesized.

Furthermore it is possible to exclude CPU time consuming instructions like multiplication, division or decimal adjust from synthesis. These are separate blocks and not part of the ALU.



## 5. Timer/Counter

Timer/Counter 0 and Timer/Counter 1 can be used as timer or as event counter. In timer mode their result is incremented every machine cycle. In counter mode it is incremented every High-Low transition at port T0 for Timer/Counter 0 or port T1 for Timer/Counter 1. The selection for “timer” or “counter” function is performed by control bits C/T in TMOD special function register.

Both – timers and counters – have four operating modes. These modes are selected by bit pairs (M0, M1) in TMOD register.

The four operating modes are:

### Mode 0

Timer 1 and Timer 0 operate as 8-bit counters (with a divide-by-32 prescaler). In this mode the timer register is configured as a 13-Bit register. The 13-Bit register consists of all 8 bits of TH0 (TH1) and the lower 5 bits of TL1 (TL1). The upper 3 bits of TL0 (TL1) are not defined.

### Mode 1

Mode 1 operates similar to Mode 0, except that the timer register is configured as 16-Bit register.

### Mode 2

In mode 2 both timer registers are configured as an 8-bit Counter (TL0 and TL1) with automatic reload. Overflow from TL0 (TL1) reloads TL0 (TL1) with the content of TH0 (TH1) preset by software. The reload leaves TH0 (TH1) unchanged.

### Mode 3

Mode 3 is different for timer 0 and timer 1. In Mode 3 timer 1 stores its counts.

A difference exists for timer 0. In Mode 3 TL0 and TH0 of timer 0 are established as two separate counters. TL0 uses the Timer 0 control bits. TH0 is locked into a timer function and takes over the use of TR1 and TF1 from timer 1. TH0 controls timer 1 interrupt release.

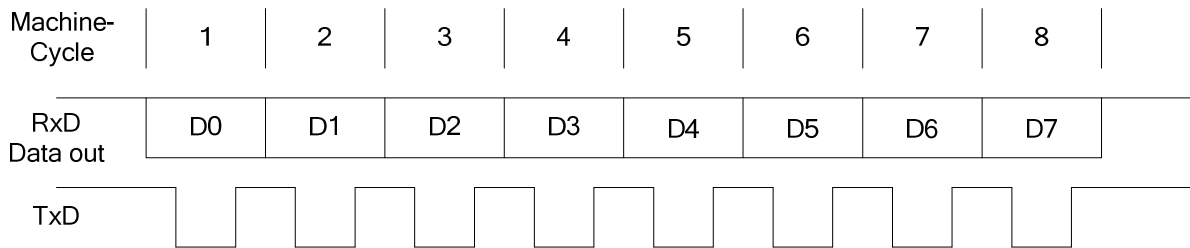
## 6. Serial Interface

The serial port is a full duplex interface. It is also receive-buffered. That means it can commence reception of a second byte before a previously received byte has been read from the register. The serial port has four operation modes. The modes are selected by bits in the special function register SCON.

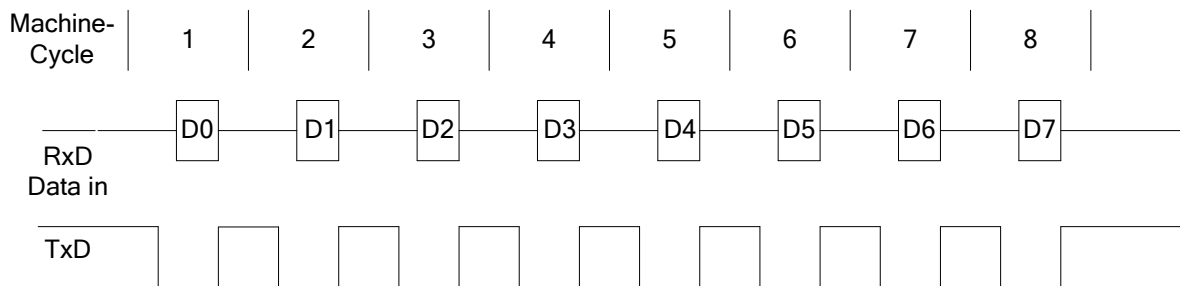
## Operating modes of the Serial Interface

### Mode 0

Serial data enters and exits through RxD. TxD provides the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the clock frequency.



**Figure 3: Transmit in Mode 0**



**Figure 4: Receive in Mode 0**

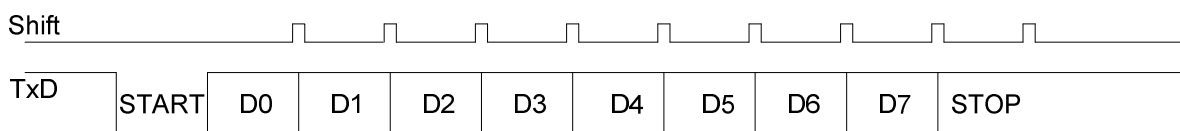
### Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). The baud rate is determined by the timer 1 overflow rate and the value of SMOD:

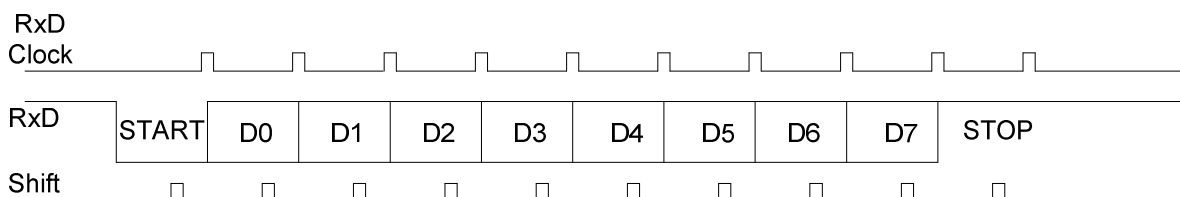
$$\text{Baud rate} = 2^{\text{SMOD}}/32 * (\text{timer-1-overflow rate})$$

If Timer 1 is in auto-reload mode the baud rate is given by the formula:

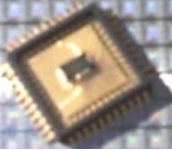
$$\text{Baud Rate} = 2^{\text{SMOD}}/32 * f_{\text{CLK}}/12 * [256 - (\text{TH1})]$$



**Figure 5: Transmit in Mode 1**



**Figure 6: Receive in Mode 1**



### Mode 2 and 3

11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 9 data bits (LSB first), and a stop bit (1). The baud rate is programmable to either 1/32 or 1/64 the clock frequency.

Mode 3 operates similar to Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

The baud rate is determined by the Timer 1 overflow rate and the value of SMOD.

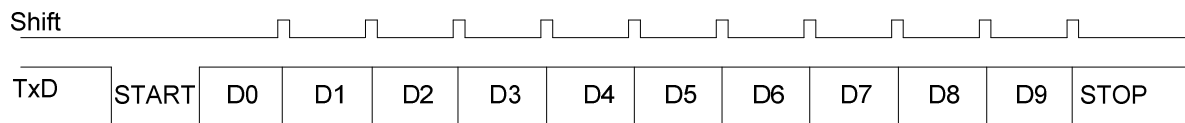


Figure 7: Transmit in Mode 2 and Mode 3

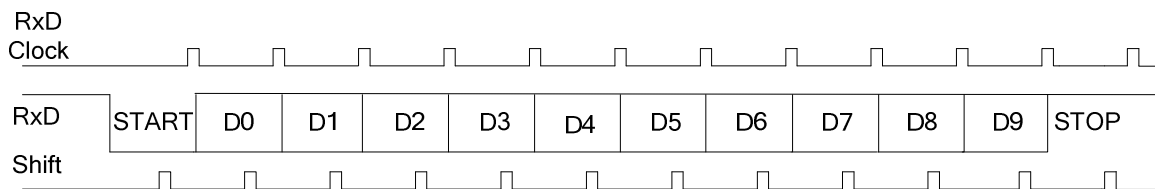
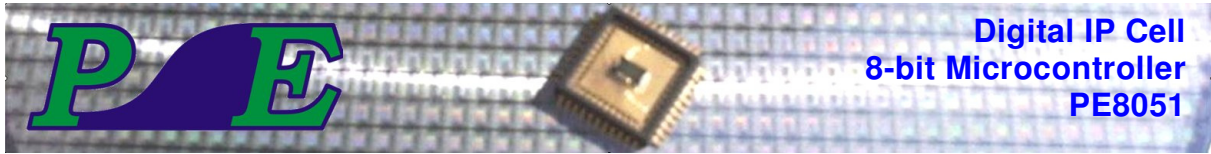


Figure 8: Receive in Mode 2 and Mode 3



## 7. Instruction register and Flow Control

The block Memory Control addresses the program memory directly. The read-in instruction is stored in the instruction register (IR) temporarily. This instruction is being decoded and initializes the flow control unit to process the commands afterwards. The control signals are generated for execution force. These signals control access to registers and memory.

## 8. Memory Control

This Block includes the special function register, the interrupt detection, the bit-addressable RAM, the instruction register and the multiplexer.

### 8.1. Bit-addressable RAM

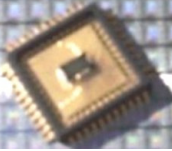
There are 128 general purpose bit-addressable locations at byte addresses 20h through 2Fh. These addresses are accessed as bytes or as bits, depending on the instruction.

### 8.2. Special-Function-Register

The SFR area covers the addresses 80h to FFh. However it is a not-connected RAM-AREA. That is why there are many unused addresses and bits.

This permits extended SFR in an ASIC implementation where additional functionality is specified.

Address	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
F8h								
F0h	B							
E8h								
E0h	ACC							
D8h								
D0h	PSW							
C8h								
C0h								
B8h	IP							
B0h	P3							
A8h	IE							
A0h	P2							
98h	SCON	SBUF						
90h	P1							
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH				PCON



### 8.3. Accumulator

The accumulator is a central register. Numerous data for arithmetic-logical operation with the CPU or data transfers run through this register.

### 8.4. B-Register

The B-register is used during multiplication and division operations. For other instructions it can be treated as another scratch pad register.

### 8.5. Program-Status-Word

The program status word contains program status information bits.

### 8.6. Stack Pointer

The stack pointer register is 8 bits wide. It contains the address of the data item currently on top of the stack. Stack operations include “pushing” data on the stack and “popping” data off the stack. Pushing on the stack increments the SP before writing data and popping from the stack reads data and then decrements the SP.

### 8.7. Data Pointer

The data pointer consists of a high byte (DPH) and a low byte (DPL). The data pointer intends for holding a 16-bit address. It may be manipulated as a 16-bit register or two independent 8-bit registers. The data pointer is used to access external code or data memory.

### 8.8. Serial Data Buffer

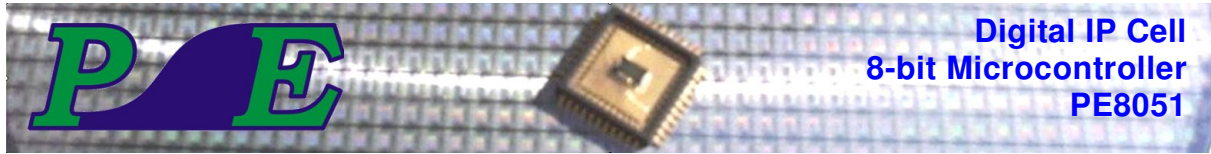
The serial buffer consists of two separate registers, a transmit buffer register and a receive buffer register. When data is moved to SBUF it goes to transmit buffer and is held for serial transmission. When data is moved from SBUF it comes from the receive buffer.

### 8.9. Timer Registers

Register pairs (TH0, TL0) and (TH1, TL1) are the 16-bit counting registers for the Timer/Counter 0 and 1.

### 8.10. Control Register for the 8051

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters and the serial interface.



## 9. Interrupt Detection

The interrupt flags sample every machine cycle. The samples are polled during the following machine cycle. If one of the flags is set the interrupt system will generate a signal which started interrupt handling.

Available interrupt sources:

1. external interrupt 0
2. timer/counter 0 overflow
3. external interrupt 1
4. timer/counter 1 overflow
5. serial interface

It is possible to add other interrupt sources in an ASIC.

## 10. Multiplexer

The multiplexer manages the access control for special function registers.

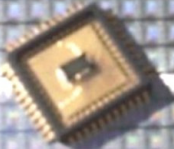
## 11. Port Control

The block port control realizes alternative functions of all ports.

## 12. Software verification on PE8051 microcontroller

The PE8051 design environment based on VHDL allows to easily convert and adapt existing software code that can be read into the ROM and can be executed in a hardware-software-co-simulation to evaluate and verify the correct command execution and peripheral access.

The PE8051 is available on FPGA platforms for hardware evaluation and system hardware design for more complex ASICs / SoC development.



For further information on availability and function please contact PE.

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