

General Description

This 10Bit successive approximation analog to digital converter employs a R2R ladder architecture to convert unipolar input voltages to a digital data word within 12 μ s with a resolution of 10Bit. Internal Offset is cancelled using auto-zero techniques. The required reference voltage generation is not included in the cell and has to be supplied external. After the external Reset signal goes "High", the first clock period is used for Signal Sampling and 11 periodes for conversion. During the next sampling phase the "valid" flag is set to "High" and the low active digital result can be read on Pin B0..B9. ADC keeps converting until the Reset signal goes "Low". The IP cell has a size of about 0,2mm².

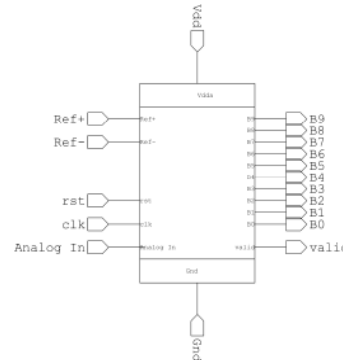
Ratings, Parameters and Conditions, typical conditions

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Operating Temperature	T _{OP}	-40	27	80	°C	
Supply Voltage	V _{DD}	3	3.3	3.6	V	
Operating Current	I _{DD}			270	μ A	
Input Voltage	V _{IN}	0.2	V _{DD} -0.8	V _{DD} -0.5	V	
Upper Reference Input	V _{ref+}	0.7	V _{DD} -0.8	V _{DD} +0.3V	V	
Lower Reference Input	V _{ref-}	0.2	0.3	V _{ref+}	V	
ADC Resolution	RES		10		Bit	
Int. Nonlinearity	INL			0.5	LSB	0.3V V _{ref-} 2.5V V _{ref+}
Diff. Nonlinearity	DNL			0.5	LSB	0.3V V _{ref-} 2.5V V _{ref+}
Conversion Time	T _{CONV}		12		μ s	

IO-Description

Interface	I/O	Function	Comment
VDDA	Input	Analog Supply	
GND	Input	Ground Supply	
Ref+	Input	Upper Reference	
Ref-	Input	Lower Reference	
rst	Input	Reset Signal	Low-active
clk	Input	External clock	Typ. 1Mhz
Analog in	Input	Analog Input	
B9..B0	Output	Digital conversion result Bits	
valid	Output	Result validation flag	

Symbol / external schematic



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