

### General Description

It is mandatory to extract a clock signal from the antenna signal to be used as logic clock for the digital core in an RFID circuit. This IP cell extracts the HF frequency (13,56MHz) from the antenna signal. The amplitude of extracted clock signal has the same high level as the digital supply voltage. The dynamic current consumption is 4uA under typical conditions. The output frequency is asymmetric and has a rectangular shape. It can be used to clock a digital core or frequency divider.

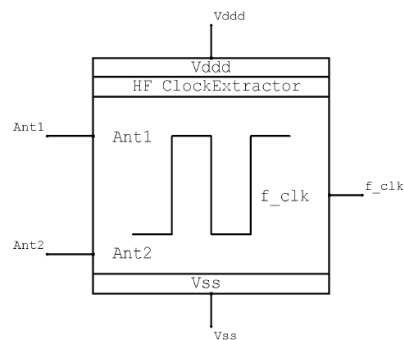
### Typical Ratings, Parameters and Condition

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Digital supply voltage	V <sub>ddd</sub>		2		V	
Supply Current	I <sub>ddd</sub>	3,9	4,0	4,2	uA	
Antenna voltage	V <sub>Ant</sub>	1,1		5,5	V	Max. voltage for initial transistors
Output Frequency	f <sub>clk</sub>	13,555	13,56	13,562	MHz	Tag frequency=13,56MHz
Duty Cycle	t <sub>H</sub>	45,3		46,1	ns	
	t <sub>L</sub>	27,5		28,6	ns	
Fall time	t <sub>fall</sub>	3,90		5,25	ns	
Rise time	t <sub>rise</sub>	3,85		4,95	ns	
Operating temperature	T <sub>op</sub>	-40	27	80	°C	

### IO-Description

Interface	I/O	Function	Comment
ANT1	Input	Antenna	Signal
ANT2	Input	Antenna	Signal
f <sub>clk</sub>	Output	Clock	Digital
V <sub>ddd</sub>	In-/Output	Supply	Digital
V <sub>ss</sub>	In-/Output	Supply	Ground

### Symbol / external schematic



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