

General Description

The digital IP Core "clock_recovery" is intended for use in ASICs with serial data input. It recovers the data clock within a digital receivers.

Features:

- Recovering the clock from a serial data stream
- 100% digital design thus technology independent
- sample data to extract the individual data bits
- useable within any Universal Asynchronous Receiver Transmitter (UART)

Ratings, Parameters and Conditions

Description language:

VHDL

Parameters:

minimal 10 bit of data stream required

system clock for recovery clock cell: $CLKX8_I \geq 8 * CLOCK_MASTER$

Frequency range:

1 – 70 MHz

Cell size (approximately):

0,1 mm² (0,6um, 2LM)

0,02 mm² (0,35um, 3LM)

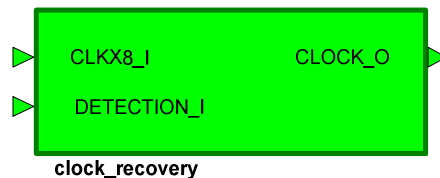
Number of ports:

3

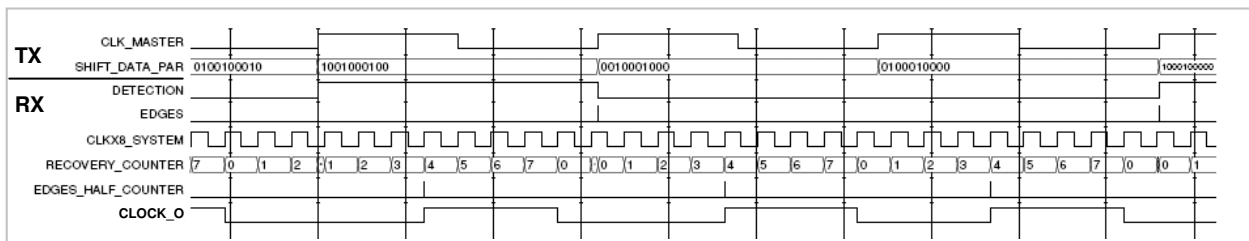
IO-Description

Interface	I/O	Function Comment
CLKX8_I	Input	System clock 8*Clock Master
DETECTION_I	Input	serial data for recovery
CLOCK_O	Output	Recovery clock

Symbol / external schematic



Cycle diagram:



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