

General Description

This incremental Sigma Delta converter provides 14 Bits of monotony. The IP cell is able to convert bipolar input voltages in the range $-V_{ref} < V_{in} < V_{ref}$ into corresponding digital output codes within 4ms (500kHz clock speed assumed). Conversion rates up to 250Hz are possible when 850 μ W of electrical power are consumed, equal to 235nJoule per Bit.

The cell contains of an additional Sample & Hold circuit, enabling input voltage sampling and pipeline conversion mode with only one pipeline stage. A digital self calibration algorithm is implemented for cancelling systematic offsets and capacitor induced non-linearity. The circuit provides high accuracy without explicit hardware trimming. The ADC can be used for sensor signal acquisition circuits where absolute conversion speed is not a key factor but power consumption is crucial.

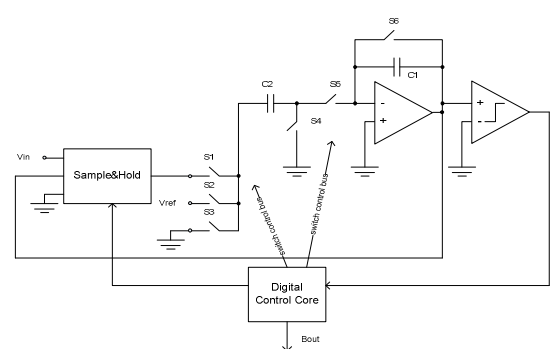
Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters:						
Supply Voltage	V_{dd}	2.7	3	3.3	V	
Supply Current	I_{dd}		250		μ A	depending on sampling frequency
Clock Speed	F_{clk}		500		kHz	other speed grades upon request
Conversion Speed	F_{conv}		250		Hz	
Input Range V_{ref} and V_{in}	V_{ref}			1	V	
Resolution after self calibration	N		14		Bits	
Absolute Maximum Ratings:						
Operating Temperature	T_{range}	-20		85	$^{\circ}$ C	
Supply Voltage	V_{dd}	-0.3		6	V	
Input Voltage	V_{in}	-0.3		$V_{dd}+0.7$		
Output Voltage	V_{out}	-0.3		$V_{dd}+0.7$		
Operating Conditions:						
Ambient Temperature	T_{amb}	-20	27	85	$^{\circ}$ C	

IO-Description

Interface	I/O	Function	Comment
GND_A, VDD_A	Input	Supply	
VMID	Input	Analogue Ground	
VREF	Input	Reference Voltage	
VIN	Input	Input voltage for AD conv.	
Bout	Outputs	Digital result	
POR_I	Input	Power On Reset	
CLK_I	Input	Clock	500kHz nom.
SOC_I	Input	Start conversion	
CALIB_I	Input	Start self-calibration	
READY_O	Output	Conversion is finished	

Block schematic



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Dieses Projekt wird im Rahmen der Technologieförderung mit Mitteln des Europäischen Fonds für regionale Entwicklung (EFRE) und mit Mitteln des Freistaates Sachsen gefördert.