

## General Description

The digital IP Core “pwire\_master” is a master protocol handler for pWire interfaces and provides a synchronous interface to pWire slaves and Dallas Semiconductor 1-Wire®, iButton® devices.

It is customizable with generic parameters for:

- speed mode
- length of transfer cycle
- period of system clock

## Ratings, Parameters and Conditions

### Description:

VHDL, EDIF

### Generic Parameters:

SPEED\_MODE\_G                      Speed mode: 0 = regular speed, 1 = overdrive speed  
 D\_WIDTH\_G                              Length of transfer cycle, Width of data port “din\_i” and “dout\_o”  
 CLK\_PERIOD\_G                          Real clock period in nanoseconds

### Frequency range:

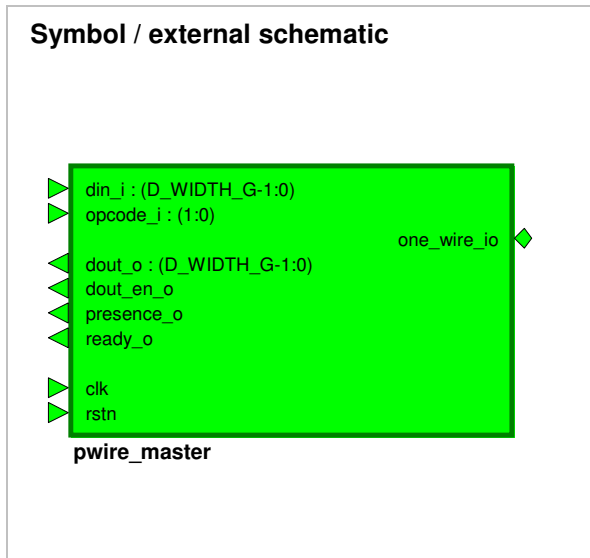
2 – 80 MHz (±30%), at regular speed  
 8 – 80 MHz (±20%), at overdrive speed

### Dimension / Area consumption (approximately):

0,18 mm<sup>2</sup> (0,6um LPower Tech. 2LM, regular speed, 8-Bit Data Width, 60 MHz),  
 0,09 mm<sup>2</sup> (0,6um LPower Tech. 3LM, overdrive speed, 8-Bit Data Width, 8 MHz).

**Number of ports:**                      8 + D\_WIDTH\_G\*2

| IO-Description |        |   |
|----------------|--------|---|
| Interface      | I/O    | Function Comment  |
| clk            | Input  | System clock  |
| rstn           | Input  | Reset (asynchrony, Lo-activ)  |
| opcode_i       | Input  | Operation (00 = NOP, 01 = Send Reset Slot, 10 = Send Data, 11 = Receive Data) |
| din_i          | Input  | Send Data Port  |
| dout_o         | Output | Recive Data Port  |
| dout_en_o      | Output | Data of Recive Data Port is current   |
| ready_o        | Output | Ready for new data transfer   |
| presence_o     | Output | Request of Reset Slot (1 = presence pulse received)                           |
| one_wire_io    | BiDi   | One Wire Port (Open Drain)  |



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