Digital IP Core
pWire Slave

General Description

The digital IP Core “pwire_slave” is a slave protocol handler for pWire interfaces and is compatible to the pWire master cell of PE as well as Dallas Semiconductor 1-Wire® and iButton® devices.

It is customizable with generic parameters for:

- speed mode
- length of transfer cycle
- period of system clock

Ratings, Parameters and Conditions

Description:
VHDL, EDIF

Generic Parameters:

SPEED_MODE_G	Speed mode: 0 = regular speed only, 1 = overdrive speed only 2 = regular and overdrive speed
D_WIDTH_G	Length of transfer cycle, Width of data port “din_i” and “dout_o”
CLK_PERIOD_G	Real clock period in nanoseconds

Frequency range:
2 – 90 MHz (±50%), at regular speed
2 – 90 MHz (±30%), at overdrive speed

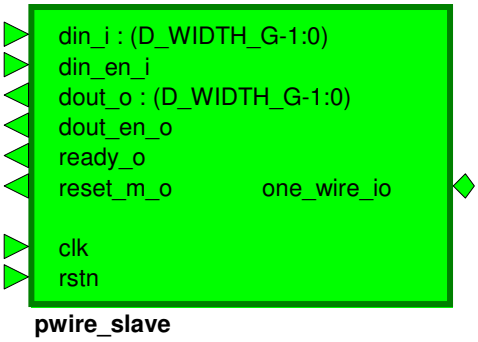
Area consumption (approximately):
0,12 mm^2 (0,6um, 3LM, regular and overdrive speed, 8-Bit Data Width, 50 MHz),
0,04 mm^2 (0,35um, 4LM, overdrive speed, 8-Bit Data Width, 2 MHz).

Number of ports: 7 + D_WIDTH_G*2

IO-Description

Interface	I/O	Function Comment
clk	Input	System clock
rstn	Input	Reset (asynchrony, Lo-activ)
din_i	Input	Send Data Port
din_en_o	Output	Send data “din_i” in next transfer cycle
dout_o	Output	Recive Data Port
dout_en_o	Output	Data of Recive Data Port is current
ready_o	Output	Ready for next transfer cycle
reset_m_o	Output	Receive reset pulse
one_wire_io	BiDi	One Wire Port (Open Drain)

Symbol / external schematic



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