



General Description

The standard cell REFSUPPLY is a versatile building block for multi chip or mainly discrete environments. It's aim is to generate, amplify and supply temperature stable and supply voltage independent voltages. The actual output voltage is selectable by the digital control bus. Step widths of 100mV give a sufficient grading for most reference purposes.

The generated voltages are buffered by an N-channel or P-channel low drop out regulator respectively, current of up to 1mA can be sourced or sunk.

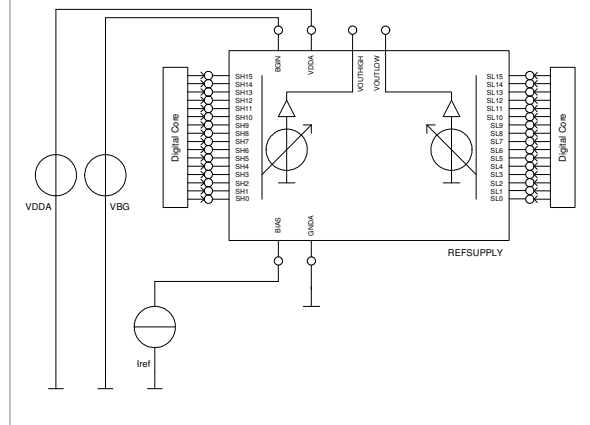
Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
Electrical Parameters:						
Supply Voltage	V_{dd}	4.75	5	5.25	V	
Supply Current	I_{gd}		1.1		mA	
Bandgap Input Voltage	V_{BG}		1.22		V	
Output Current	I_{out}		300	1000	μ A	
Lower Output Voltage	V_{outlow}	0.5		2	V	100mV step width
Upper Output Voltage	$V_{outupper}$	3		4.5	V	100mV step width
Minimum Load Capacitance	$C_{loadmin}$	100			pF	external capacitor for voltage buffering
Power Supply Rejection	PSRR		60		dB	PSRR of bandgap voltage supply. Actual PSRR is depending on size of employed load capacitors.
Absolute Maximum Ratings:						
Operating Temperature	T_{range}	-20		80	$^{\circ}$ C	
Supply Voltage	V_{dd}	-0.3		7	V	
Input Voltage	V_{in}	-0.3		$V_{dd}+0.7$		
Output Voltage	V_{out}	-0.3		$V_{dd}+0.7$		
Operating Conditions:						
Ambient Temperature	T_{amb}	-20	27	80	$^{\circ}$ C	

IO-Description

Interface	I/O	Function	Comment
GNDA	Input	Supply	
VDDA	Input	Supply	
BIAS	Input	reference current	
BGIN	Input	reference voltage	derived from bandgap
SL0-SL15	Input	lower voltage control bus	
SH0-SH15	Input	upper voltage control bus	
VOUTLOW	Output	lower voltage output	
VOUTHIGH	Output	upper voltage output	

Symbol / external schematic



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Dieses Projekt wird im Rahmen der Technologieförderung mit Mitteln des Europäischen Fonds für regionale Entwicklung (EFRE) und mit Mitteln des Freistaates Sachsen gefördert.