



## General Description

The analogue IP cell RelaxOSC XC10LV is a relaxation oscillator optimized for low supply voltage operation and low power consumption. Because of its supply voltage range it can be used in single battery cell operated designs.

The cell is designed for a nominal operation frequency of 1.66MHz and can be trimmed to this value using a 4Bit wide trim input. In typical application, Poly-Si fuse cells are used a non-volatile memory holding the trim information.

An enable input is implemented to power down the cell is the clock is not needed. Else two non-overlapping clock signals are generated with a very short start up time.

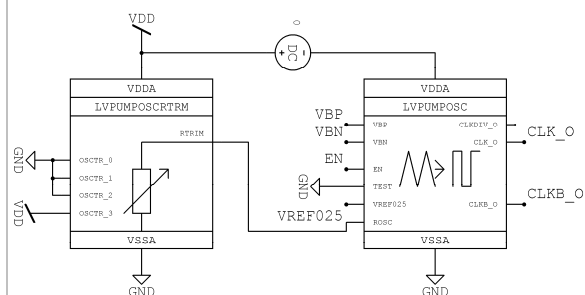
## Ratings, Parameters and Conditions

Parameter / Condition	Symbol	Min	Typ.	Max	Unit	Comment
<b>Electrical Parameters:</b>						
Supply Voltage	V <sub>dd</sub>	1.3	1.55	1.6	V	
Active Supply Current	I <sub>dd</sub>	6	12	22	µA	depending on output frequency
Inactive Supply Current	I <sub>ddidle</sub>			25	nA	
Frequency Trimming Range typical case	F <sub>CLKTRIM</sub>	1	1.66	2.5	MHz	
Frequency Accuracy trimmed over Voltage and Temperature	F <sub>CLKTM</sub>	1.62	1.66	1.73	MHz	trimmed to 1.66MHz, typical case
Power Up Time	T <sub>SU</sub>			100	µs	
Clock Duty Cycle	DC <sub>CLK</sub>	45	48	60	%	
<b>Absolute Maximum Ratings:</b>						
Operating Temperature	T <sub>range</sub>	-40		140	°C	
Supply Voltage	V <sub>dd</sub>	-0.3		6	V	
Input Voltage	V <sub>in</sub>	-0.3		V <sub>dd</sub> +0.7		
Output Voltage	V <sub>out</sub>	-0.3		V <sub>dd</sub> +0.7		
<b>Operating Conditions:</b>						
Ambient Temperature	T <sub>amb</sub>	-20	27	80	°C	

## IO-Description

Interface	I/O	Function	Comment
VSSA	input	Supply	
VDDA	Input	Supply	
OSCTR_0-3	Inputs	Trim Inputs	
VREF025	Input	Reference Voltage Input	nom. 150mV
EN	Input	Enable Sig.	
VBN	Input	N Bias Voltage	
VBP	Input	P Bias Voltage	
TEST	Input	Test enable	
CLKDIV_O	Output	FCLK/1024	only active when Test=H
CLK_O	Output	Clock Output	
CLKB_O	Output	inverted Clock Output	

## Block schematic, ext. component diagram



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