General

The PE5002 is a 100-channel, 10Bit capacitive sensor signal acquisition circuit. It comprises of all the stages needed for synchronous evaluation (amplification, rectification, A-to-D conversion) of small AC currents in the frequency range 1MHz to 10MHz. Each of the circuit stages is implemented once per input line. Data memory provides a 10bit wide serial data stream. Several setup prcedures and external signals are required for proper operation. One way of system implementation is presented in this document. The control of the PE5002 can also be implemented employing the control IC PE5003. The sensor element can also stimulated with IC PE5001.

PE5002 controlled by an external microcontroller

The PE5002 can be used for the acquisition of a line consisting with 100 capacitive sensors. One way of system implementation can be accomplished with a standard microcontroller and some passive components. For a detailed description of the PE5002 please refer to the PE5002 data sheet on the www.pe-gmbh.com web site. It is essential to understand the PE5002 internal circuitry before implementing a complete sensor system.

Block diagram

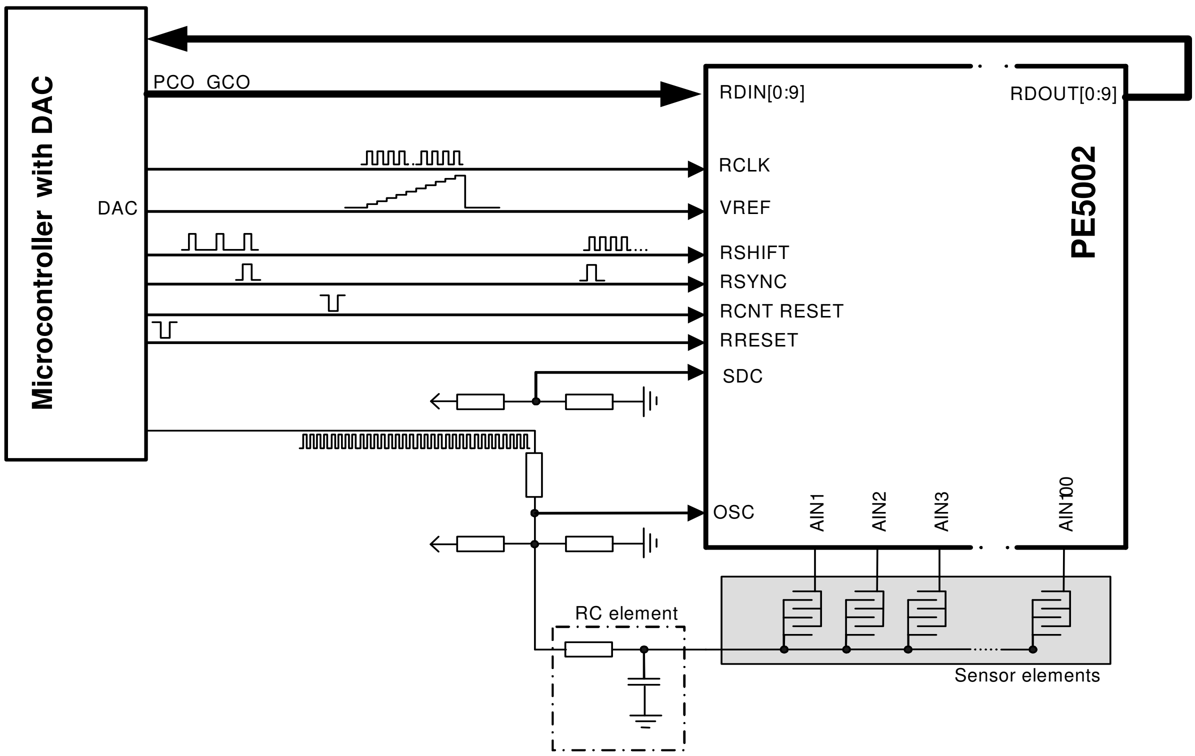

Figure 1: Block diagram

To use the function of the PE5002 the capacitive sensor elements must be stimulated by an AC current. This can ideally be accomplished with a sine-wave signal as it is provided by the PE5003. Another simpler way as represented in the block diagram in Figure 1 with a saw-tooth signal, which is generated over an RC element from a square wave signal.
The peak-to-peak voltage for the sensor elements to the analog sensor inputs
AIN1 - AIN100 of the PE5002 should be within the range of 0,5V to 2V in order to remain in the transducer range of the AD-converter.
Parameters of the RC element must be adapted accordingly to match frequency and capacitive characteristics of the sensor elements. The PE5002 needs a reference signal at the OSC input for correct "lock-in-detection". This signal must have exactly the same frequency as the stimulating signal for the sensor elements. Therefore it is necessary to generate both signals from the same source. The OSC signal can have rectangular or saw-tooth shape.

The voltage range should be between
V_{SDC} - 0,05V and V_{SDC} + 0,05V.
The sensor signal acquisition is carried out by amplification of a capacitance dependent input current by a trans-impedance amplifier and synchronous rectification. The resulted DC signal is converted by an ADC into a 10bit binary value. The PE5002 needs a linear voltage ramp at VREF input which serves as reference value for the comparators of the ADCs. The number of steps of this voltage ramp partially defines the resolution of the system. Additionally for each ramp step a clock pulse at the input RCLK for the counter of the ADCs is required. The voltage ramp can be generated directly by a DAC in the microcontroller, if available. It can also be generated by an additional DAC or from an R2R-network being driven by one or more ports of the microcontroller. It has to be synchronous with the other signals RCNTReset, RShift and RSynch as depicted in Figure 3.
If more than 100 sensors have to be converted multiple PE5002 can be connected in a row.

Partial block : Initialization (Figure 3)

The low active reset at the input RRESET clears the contents memory register structure (Figure 2) as well as contents of registers PCO (Figure 4) and GCO (Figure 5). Now the new values for the registers PCO and GCO must be loaded. First the value for GCO must be pushed in place 2 and than PCO in place 1 in the register chain and through the multiplexer switch by RSYNC and by a clock pulse at RSHIFT the values be loaded into the registers DPCO and DGCO. Later these registers will overwrite by counting register contents of the ADCs, than they must be loaded again.

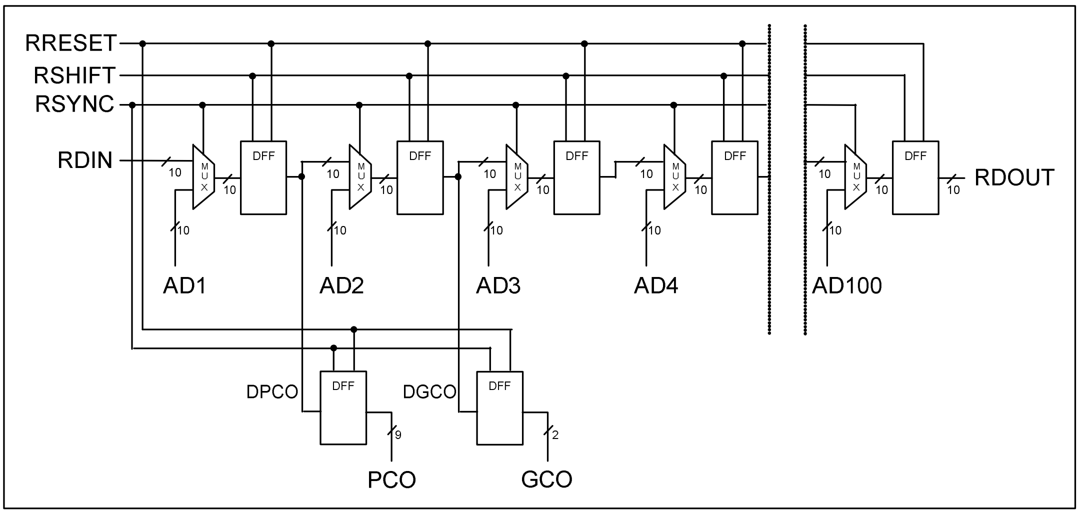

Figure 2: Shift registers structure as data memory

Flow chart

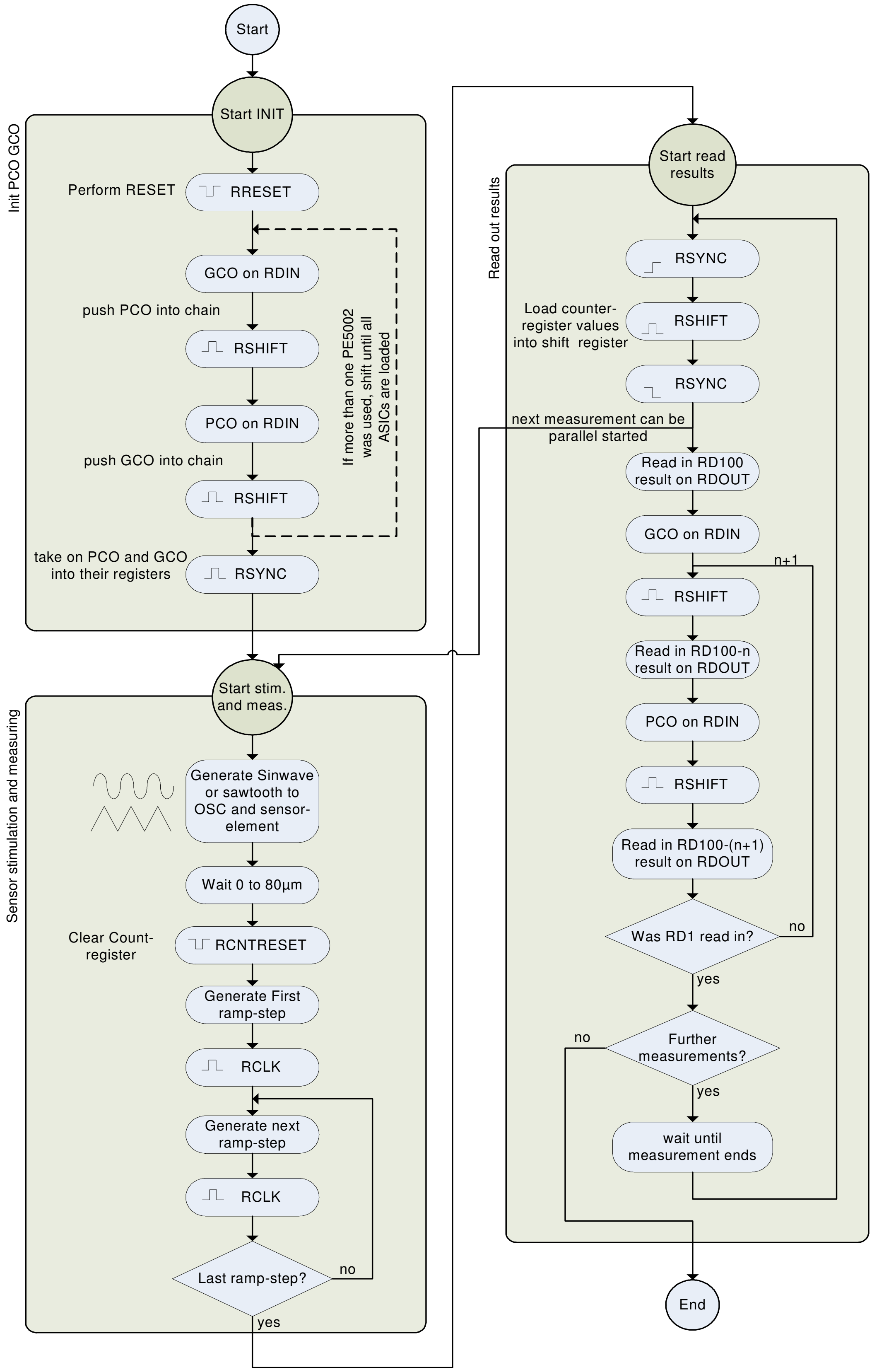

Figure 3: Flow chart

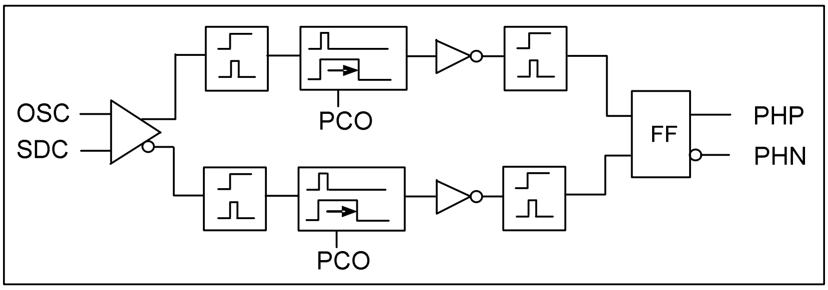

Figure 4: Phase shifter

PCO definition:

```
Delay:      typical for one LSB 3ns
Format:     RDIN[9:0] <= "XPPPPPPPPP"
                           | | |---------------|   - Phase shifter delay PCO[7:0]
                           | |                     - Phase inverter PCO[8] (phase switch 180°; with '1')
                           |                       - ignored value

Example:    RDIN[9:0] <= "0000000001"             - 3ns Phase shifting (positive)
            RDIN[9:0] <= "0011111111"             - 768ns Phase shifting (positive)
            RDIN[9:0] <= "0100000001"             - 3ns Phase inverse shifting (negative)
```

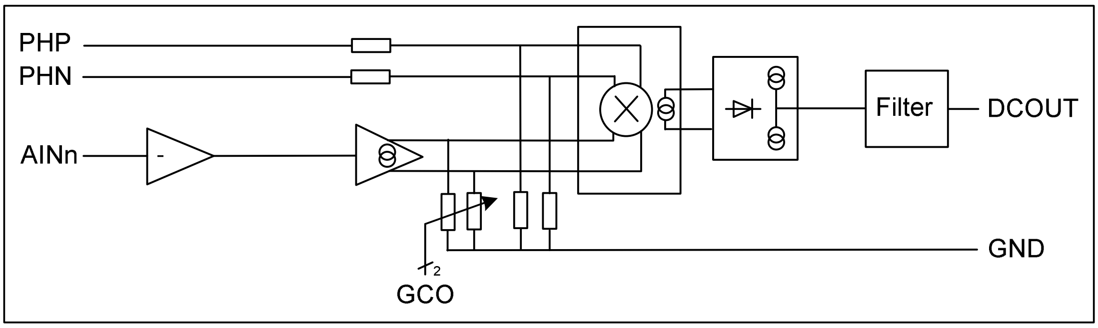

Figure 5: Input signal path

GCO definition:
Format: RDIN[9:0] <= "XXXXXXXXGG"
X = ignored value
GG = GCO[1:0]

GCO[1:0]	Gain / V
"00"	3.03
"01"	3.27
"10"	3.35
"11"	3.73

Partial block : Stimulation and measurement (Figure 3)

The settling time after the sensor chain has been stimulated depends on the stimulation frequency, the characteristics of the sensor element and the turn on time of the comparator in the PE5002. The contents of the individual counting register memory must be erased by a "Low" pulse at the input RCNTRESET before the voltage ramp can start. The ramp voltage rises. It will reach a voltage level which is greater than the DC value generated from the sensor input. At this point the comparator generates a stop signal and the actual counter value is transferred to the appropriate counting register. The counter clock is supplied on RCLK (Figure 6).

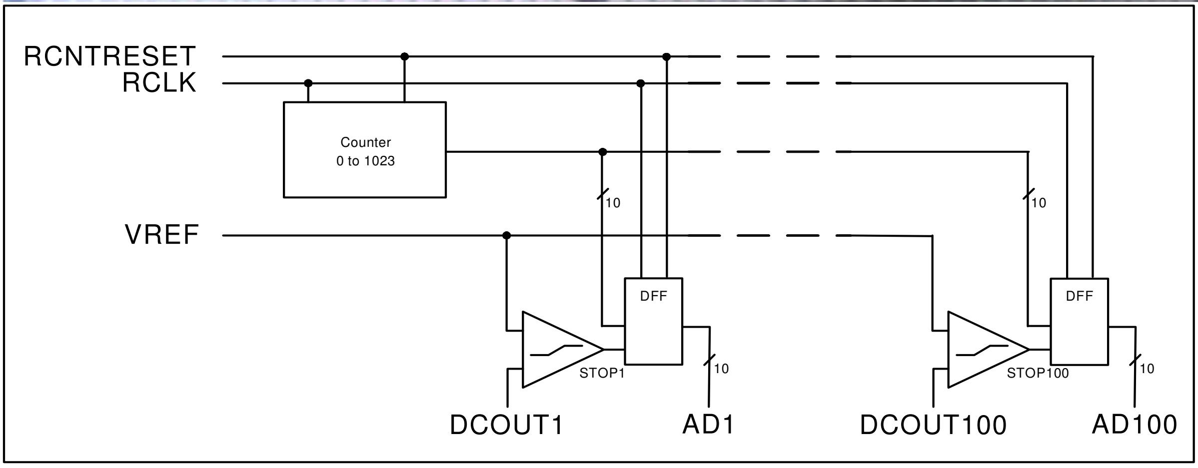

Figure 6: Analog-to-digital conversion

Partial blocks : Read out results (Figure 3)

After the measurement is finished, every counting register has stored one value. Now these values must be transferred by RSYNC and RSHIFT to the memory register. The values can be pushed out over the 10Bit output RDOUT by clocks at RSHIFT. At the same time new values for PCO and GCO can be pushed into the PE5002.

Contact Addresses

Germany

Stuttgart

Productivity Engineering
Process Integration GmbH
Behringstrasse 7
D-71083 Herrenberg
Germany
Phone.: +49 (0) 70322798 0
Fax: +49 (0) 70322798 29
Email: info@pe-gmbh.com

Dresden

Productivity Engineering GmbH
Branch
Sachsenallee 9
D-01723 Kesselsdorf
Germany
Phone.: +49 (0) 3520490 207
Fax: +49 (0) 3520490 270
Email: info@pe-gmbh.com

This project was supported by Award No. 2005-IJ-CX-K067 awarded by the National Institute of Justice, Office of Justice Programs, US Department of Justice. The opinions, findings, and conclusions or recommendations expressed in this publication/program/exhibition are those of the author(s) and do not necessarily reflect the views of the Department of Justice.